UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,315	08/15/2003	William D. Sawyer	CSLL-662CP (56247-235)	2855

7590 01/26/2005

Mark G. Lappin, P.C.
McDermott, Will & Emery
28 State Street
Boston, MA 02109

EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,315	SAWYER ET AL.	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-31* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the application filed 8/15/03.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-30drawn to a method for making a semiconductor device, classified in class 438, subclass 411.

   II. Claim 31, drawn to a semiconductor device, classified in class 257, subclass 417.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case a SOI wafer may be grown/deposited on a substrate rather than bonding a SOI wafer on a substrate.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mark G. Lappin on 12/28 a provisional election was made without oral traverse to prosecute the invention of group I, claims 1-30. Affirmation of this election must be made by applicant in replying to this Office action. Claim 31 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-3, 5-9, and 23 are rejected under the judicially created doctrine of double patenting over claims 1-3, 4 and 6-8, and 9 of U. S. Patent No. 6,677,694 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: all of the positive steps of claims 1-3, 5-9, and 23 are recited in the cited claims of 6,677,694.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3, 5-9, 11, 13-15, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hays (US 006277666).

Hays teaches all of the positive steps of claims 1-3, 5-9, 11, 13-15, and 23-24 as follows.

Regarding claim 1, Hays teaches a handle wafer (34), a dielectric layer (36), a device layer (38), a mesa etch (14, figure 1a), a substrate (30) with a pattern formed in the substrate, bonding the two wafers (figure 2c), removing the handle (figure 2d), and performing a structural etch (50).

Regarding claim 2, the dielectric layer of the SOI comprises silicon dioxide (column 6 line 1).

Regarding claim 3, the structural etch is a deep (figure 2b) reactive ion etch (column 7 lines 29-30).

Regarding claim 5, the substrate is glass (column 6 line 10).

Regarding claim 6, the substrate is glass (column 6 line 10) and the pattern comprises multilevel metallization (44 and 48).

Regarding claim 7, the substrate is a recess etched glass wafer (figure 2b, column 6 line 10).

Regarding claim 8, a blanket sputter of the multilevel metallization is performed and excess metal not directly applied to the substrate is lifted off (column 6 line 43 to column 7 line 14).

Regarding claim 9, the bonding of the wafers is anodic (column 2 lines 38-43).

Regarding claim 11, the dielectric layer is removed by a dry plasma etch (column 8 line 3, RIE is a dry etch).

Regarding claim 13, the structural etch is straight down through the device layer to the substrate (figure 2b).

Regarding claim 14, the device layer is removed a locus where the structural etch is preformed, so that when the device layer is bonded to the substrate, the surface of the device layer is spaced apart from the substrate (figure 2c).

Regarding claim 15, the substrate includes a patterned metal layer, the metal layer defining gaps that are positioned other than under operable elements (figure 2c).

Regarding claim 23, in addition to the limitations recited toward claim 1, Hays teaches this method for forming an accelerometer (column 9 lines 22-27).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hays (US 006277666) in view of Sawada (US 006413714).

Hays teaches all of the positive steps of claim 4 as recited above in regard to claim 1, except for the access port.

Sawada teaches the method that includes an access port to optimize operation.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Hays by including an access port as taught by Sawada for optimum operation.

12. Claims 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hays (US 006277666) in view of Fukada (US006077721A) or Clark (US006433401B1).

Hays teaches all of the positive steps of claims 16 and 24 as recited above in regard to claim 1, except for bonding the SOI wafer and the substrate at a predetermined pressure less than 1 atmosphere.

Regarding claim 16, Hays is silent as to the pressure of bonding the two pieces. Fukada bonds the two pieces by anodic bonding (as in the instant application) and teaches that a vacuum is maintained in the through holes, (column 8 line 67 to column 9 line 2), suggesting that the anodic bonding is preformed in a vacuum (less than 1 atmosphere pressure, standard pressure). Clark also teaches bonding of two wafers by anodic bonding and teaches that the bonding is in a partial vacuum (column 7 lines 40-52). Thus is in known to perform anodic bonding at pressures below 1 atmosphere. Regarding the term "predetermined", it is assumed that anyone performing a process uses predetermined parameters, and that the process is not random.

Regarding claim 24, Hays teaches a handle wafer (34), a dielectric layer (36), a device layer (38), a mesa etch (14, figure 1a), a substrate (30) with a pattern formed in the substrate, bonding the two wafers (figure 2c), removing the handle (figure 2d), and performing a structural etch (50). Hays is silent as to the pressure of bonding the two pieces. Fukada bonds the two pieces by anodic bonding (as in the instant application) and teaches that a vacuum is maintained in the through holes, (column 8 line 67 to column 9 line 2), suggesting that the anodic bonding is preformed in a vacuum (less than 1 atmosphere pressure, standard pressure). Clark also teaches bonding of two wafers by anodic bonding and teaches that the bonding is in a partial vacuum (column 7

lines 40-52). Thus is in known to perform anodic bonding at pressures below 1 atmosphere. Regarding the term "predetermined", it is assumed that anyone performing a process uses predetermined parameters, and that the process is not random.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Hays by utilizing anodic bonding as taught by Fukada and Clark to be preformed in vacuums (less than 1 atmosphere).

13. Claims 10, 12, 17-20 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hays (US 006277666) in view of McCarthy (US 005760443). Hays teaches all of the positive steps of claims 10, 12, 17-20, and 25-28 as recited above in regard to claim 1, except for removing the handle wafer by a wet chemical etch and that the substrate comprises a SOI wafer.

Regarding claim 4, Hays removes the handle wafer by RIE (column 8 line 1). McCarthy teaches removing the handle wafer by polishing or by wet/dry (RIE) techniques giving them an art recognized equivalence.

Regarding claim 12, McCarthy teaches the substrate may be a glass substrate or wafer or insulated wafer (SOI) (column 3 lines 15, and 30-31) giving them an art-recognized equivalence.

Regarding claim 17, Hays teaches removing the handle wafer but does not teach removing it in two steps. McCarthy teaches removing the handle wafer by polishing, or by a multiple etch step. The wafer (being a SOI wafer) is multiple layers. McCarthy teaches wet etching with KOH and then by plasma etch with SF6 and removing any remaining material (a thin layer) by XeCl to produce a very smooth surface (column 5 lines 8-40).

Regarding claim 25, in addition to the limitations discussed above (see claim 1), as McCarthy teaches a multiple step etch, McCarthy teaches removing the handle wafer to a predetermined distance from the dielectric layer by a first etchant and removing the thin remaining portion by a second etchant.

Regarding claims 18 and 26, the first etchant is a relatively fast etchant (McCarthy does not cite etch rate in relative terms only in material etched/minute (2500 angstroms/minute), but the etchant is identical to that of the instant application, therefore the etch rate would be the same.

Regarding claims 19 and 27, the second (final) etchant is a relatively slow etchant (McCarthy does not cite etch rate, but the etchant is in the same class Xe-halogen) as that of the instant application, therefore the etch rate would be the same.

Regarding claims 20 and 28, the first etchant is KOH (column 5 line 19).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Hays by including a SOI wafer and removing the handle wafer by known removal techniques as taught by McCarthy.

14. Claims 22 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hays (US 006277666) in view of McCarthy (US 005760443) and in further view of Clark (US006291875).

Hays teaches all of the positive steps of claims 10, 12, 17-20, and 25-28 as recited above in regard to claim 1, except for removing the handle wafer by a wet etch of TMAH. Hays is silent as to the removal methods. McCarthy teaches a wet etchant of KOH and a Xe-halogen. Clark teaches removal of the handle wafer by KOH, TMAH, or dry etch, giving them an art recognized equivalence. Further, the instant specification teaches TMAH and a dry etch with Xe-halogen, without teaching any criticality between the two (page 9, paragraph 43).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or of any unexpected results arising there from. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in the claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1515, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Hays and McCarthy by etching with TMAH as taught by Clark to be an art recognized equivalent.

15. Claims 21 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hays (US 006277666) in view of McCarthy (US 005760443) and in further view of Fedder (US 006458615).

Hays and McCarthy teach all of the positive steps of claims 21 and 29 as recited above in regard to claims 17 and 25, except for removing the handle wafer by XeF2. McCarthy uses second etches of SF6 or XeCl. Fedder teaches etching the wafer with SF6 or XeF2 giving them an art recognized equivalence.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Hays and McCarthy by etching with XeF2 as taught by Fedder to be an art recognized equivalent.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

January 24, 2005